

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1-3 (Cancelled).

4. (Currently Amended) ~~An insulated A trench-gate~~
type semiconductor device comprising:

a first semiconductor region selectively formed in a
semiconductor substrate;

a second semiconductor region selectively formed in
said first semiconductor region;

a trench which is reached extending from a major
surface of said second semiconductor region to said
semiconductor substrate; and

a first conductive layer which is formed via an
insulating film in said trench; wherein:

~~a gate pillar, which is constituted by including
portions of said first conductive layer and a cap
insulating film for capping an upper surface of said first
conductive layer owns a pillar which is elongated on, said
gate pillar projecting from a major surface of said second
semiconductor region;~~

a side wall spacer is provided formed on a side wall of the pillar of a projecting portion of said gate pillar;

a contact hole, formed by an etching process using
said side wall spacer as a mask, said contact hole
extending from said major surface of said second
semiconductor region toward said first semiconductor
region; and

an electrode is connected to said second semiconductor
region in a contact region which is defined by said side
wall spacer; and

a second conductive layer, formed in said contact hole
and over said semiconductor substrate, said second
conductive layer being connected to an electrode; and

wherein said semiconductor substrate is used as a
drain, said first conductive layer is used as a gate, and
said second semiconductor region is used as a source.

5. (Currently Amended) An insulated A trench-gate
type semiconductor device comprising:

a first semiconductor region selectively formed in a
semiconductor substrate;

a second semiconductor region selectively formed in
said first semiconductor region;

a trench which is reached extending from a major surface of said second semiconductor region into said semiconductor substrate; and

a first conductive layer which is formed via an insulating film in said trench; wherein:

a portion of said conductive layer owns a pillar,
including a portion of said first conductive layer, which
is elongated on said pillar projecting from the [[a]] major
surface of said second semiconductor region;

a side wall spacer is provided formed on both a side wall of the said pillar of said conductive layer and also a side wall of a cap insulating film for capping an upper surface of said first conductive layer;

a contact hole, formed by an etching process using
said side wall spacer as a mask, said contact hole
extending from the major surface of said second
semiconductor region toward said first semiconductor
region; and

an electrode is connected to said second semiconductor
region in a contact hole formed in a contact region which
is defined by said side wall spacer; and

a second conductive layer, formed in said contact hole
and over said semiconductor substrate, said second
conductive layer being connected to an electrode; and

wherein said semiconductor substrate is used as a drain, said first conductive layer is used as a gate, and said second semiconductor region is used as a source.

6. (Currently Amended) An insulated A trench-gate type semiconductor device as claimed in claim 4, wherein: said first conductive layer which constitutes the gate is includes polycrystal silicon, , and said insulating film is a includes thermal oxide film.

7. (Currently Amended) An insulated A trench-gate type semiconductor device comprising:

a first conductivity type semiconductor main body;
a second conductivity type first semiconductor region formed at a predetermined depth within one major surface of said semiconductor main body, said second conductivity type being opposite to said first conductivity type;

a first conductivity type second semiconductor region formed at a predetermined depth within said first semiconductor region;

a first trench, which penetrates said first semiconductor region, and is reached said first trench extending from a major surface of said second semiconductor region to said semiconductor main body;

a gate pillar gate, which is constituted by both
including a gate-purpose conductive layer embedded via an
insulating film into said first trench and a cap insulating
film for capping an upper surface of said gate-purpose
conductive layer, and a portion of which said gate pillar
gate having a pillar portion project[[ed]]ing from the
major surface of said second semiconductor region; and
a side wall spacer formed on a side wall of the
projecting portion of said gate pillar;

a contact hole, formed by an etching process using
said side wall spacer as a mask, said contact hole
extending from said second semiconductor region into said
first semiconductor region; and

a conductive layer which is formed in said contact
hole and on a semiconductor substrate and which is
connected to a first electrode.

a first electrode which is electrically connected to
said second semiconductor region in a region between a side
wall spacer provided on a side wall of said pillar portion
of the pillar gate, and said side wall spacer.

8. (Currently Amended) An insulated A trench-gate
type semiconductor device comprising:

a first conductivity type semiconductor main body;

a second conductivity type first semiconductor region formed at a predetermined depth within ~~one major surface of~~ said semiconductor main body, said second conductivity type being opposite to said first conductivity type;

a first conductivity type second semiconductor region formed at a predetermined depth within said first semiconductor region;

a first plurality of first trenches which penetrates said first semiconductor region, and ~~are reached~~ extends from a major surface of said second semiconductor region into said semiconductor main body;

a conductive layer, for a gate, embedded via an insulating film into each of said first plurality of trenches, said conductive layer including a plurality of pillar portions projecting from said major surface of said second semiconductor region, each pillar portion having an upper surface capped with an insulating film;, and a portion of which ~~said conductive layer for said gate owns a pillar portion projected from the major surface of said second semiconductor region~~

a plurality of side wall spacers provided formed on a respective side walls of said plurality of pillar portions and also a side wall of a said cap insulating films for capping an upper surface of said pillar portion;

a second plurality of second trenches, which are made shallower than said first plurality of trenches, and are formed in such a manner that said second trenches are reached extending from the said major surface of the said second semiconductor region into said first semiconductor region between said side wall spacers located adjacent to each other; and

a first electrode source-region conductive layer, which is embedded into each of said plurality of second trenches, so as to be to electrically connect[[ed]] to said first semiconductor region and said second semiconductor region to a first electrode; and which is commonly connected on said conductive layer for said gate.

a second electrode, for a drain, formed on a rear surface of said semiconductor main body.

9. (Currently Amended) An insulated A trench-gate type semiconductor device as claimed in claim [[7]] 8, wherein:

said conductive layer for said gate is made of includes a polycrystal silicon containing an impurity;

said first electrode is made of a includes a first metal which contains aluminium having aluminum as a major component; and

said second electrode is made of a includes a second
 metal material different from said first metal material of
 the first electrode.

10. (Currently Amended) An insulated A trench-gate
 type semiconductor device as claimed in claim 7, further
comprising wherein:

a said second electrode, is formed on another major
 surface of said semiconductor main body, which is located
 opposite to said major surface of said semiconductor body,
 thereof; and said second electrode is made of either
 including a metal layer in which nickel, titanium, nickel,
 and silver are sequentially stacked, or another metal layer
 in which titanium, nickel, and gold are sequentially
 stacked.

11. (Currently Amended) An insulated A trench-gate
 type semiconductor device as claimed in claim 10, wherein:
 said first electrode is a source electrode; and
 said second electrode is a drain electrode.

12. (Currently Amended) An insulated A trench-gate
 type semiconductor device as claimed in claim [[7]] 8,
 wherein:

wherein said first plurality of trenches are formed in
 a stripe shape in such a manner that a side surface of said

first semiconductor region constitutes either includes a crystalline surface (100) or a surface equivalent to said crystalline surface (100), and

wherein carriers are move[[d]] along either said crystalline surface (100) or said surface equivalent to said crystalline surface (100) under influence of by an electric field of said conductive layer ~~for said gate~~.

13. (Currently Amended) An insulated A trench-gate type semiconductor device as claimed in claim [[7]] 8, further comprising wherein:

a field insulating film, is formed on a portion of the said major surface of said semiconductor main body;

an extension portion of said conductive layer, for said gate is provided formed on a portion of said field insulating film; and

a third electrode, made of the same material as that of said first electrode is connected to said extension portion of said conductive layer for said gate.

14. (Currently Amended) An insulated A trench-gate type semiconductor device as claimed in claim 13, wherein: a back-to-back protective element, which is electrically connected between said first electrode and

said third electrode, is provided formed on another portion of said field insulating film.

15-17 (Cancelled).

18. (Withdrawn) A method for manufacturing an insulated-gate type semiconductor device in which a gate-purpose conductive layer is embedded into a trench which is formed in a semiconductor substrate, and a source-purpose conductive layer is provided on said major surface, comprising:

a step for forming a first semiconductor region within said semiconductor substrate;

a step for forming a trench in said semiconductor substrate in such a manner that said trench penetrates said first semiconductor forming region;

a step for forming a gate insulating film on a surface of said first semiconductor region which is exposed within said trench;

a step in which the trench where said gate insulating film is formed by a gate pillar made of both said gate-purpose conductive layer and a cap insulating film for capping an upper surface of said gate-purpose conductive layer, and a portion of said gate pillar is projected from the major surface of said semiconductor substrate;

a step for forming a second semiconductor region within said first semiconductor region which is segmented by said trench;

a step for forming a side wall spacer on both said projected conductive layer and an insulating film for covering an upper surface of said projected conductive layer; and

a step for forming said source-purpose conductive layer in a source contact region defined by said side wall spacer.

19. (Withdrawn) A method for manufacturing an insulated-gate type semiconductor device in which a gate-purpose conductive layer is embedded into a trench which is formed in a semiconductor substrate, and a source-purpose conductive layer is provided on said major surface, comprising:

a step for forming a first semiconductor region within said semiconductor substrate;

a step for forming a plurality of trenches in said semiconductor substrate in such a manner that said trenches penetrate said first semiconductor forming region;

a step for forming a gate insulating film on a surface of said first semiconductor region which is exposed within each of said trenches;

a step in which each of said trenches where said gate insulating film is formed is embedded, and a portion of said gate-purpose conductive layer which is projected to the major surface of the semiconductor substrate is formed;

a step for forming a second semiconductor region within said first semiconductor region which is segmented by said trenches;

a step for forming a side wall spacer on both said projected conductive layer and an insulating film for covering an upper surface of said projected conductive layer;

a step for forming a contact hole in a source contact region defined by said side wall spacer; and

a step for forming said source-purpose conductive layer in said contact hole.

20. (Withdrawn) A method for manufacturing an insulated-gate type semiconductor device in which a gate-purpose conductive layer is embedded into a trench which is formed in a semiconductor substrate, and a source-purpose

conductive layer is provided on said major surface,
comprising:

 a step for forming a first semiconductor region within
 said semiconductor substrate;

 a step for forming a trench in said semiconductor
 substrate in such a manner that said trench penetrates said
 first semiconductor forming region;

 a step for forming a gate insulating film on a surface
 of said first semiconductor region which is exposed within
 said trench;

 a step in which the trench where said gate insulating
 film is formed by a gate pillar made of both said
 conductive layer for said gate and a cap insulating film
 for capping an upper surface of said conductive layer for
 said gate, and a portion of said gate pillar is projected
 from the major surface of said semiconductor substrate;

 a step for forming a second semiconductor region
 within said first semiconductor region which is segmented
 by said trench;

 a step for forming a side wall spacer on both said
 projected conductive layer and an insulating film for
 covering an upper surface of said projected conductive
 layer;

a step for forming a contact hole in said second semiconductor region, while said side wall spacer is employed as a mask;

a step in which after said contact hole has been formed, the side wall spacer is moved backwardly by way of an etching back operation so as to expose a surface of the semiconductor substrate of said second semiconductor region; and

a step for forming said source-purpose conductive layer within both the exposed surface portion of the semiconductor substrate of said second semiconductor region and also said contact hole.

21. (New) A trench-gate type semiconductor device as claimed in claim 7, further comprising:

a second electrode, formed on another major surface of said semiconductor main body, said second electrode located opposite to said major surface of said semiconductor body and said second electrode including a metal layer in which nickel, titanium, nickel, and silver are sequentially stacked.

22. (New) A trench-gate type semiconductor device, comprising:

a first conductivity type semiconductor main body;

a second conductivity type first semiconductor region formed at a predetermined depth within said semiconductor main body, said second conductivity type being opposite to said first conductivity type;

a first conductivity type second semiconductor region formed at a predetermined depth within said first semiconductor region;

a first trench which penetrates said first semiconductor region, said first trench extending from a major surface of said second semiconductor region into said semiconductor main body;

a gate pillar, including portions of a conductive layer embedded via an insulating film into said first trench and a cap insulating film capping an upper surface of said conductive layer, said gate pillar having a portion projecting from the major surface of said second semiconductor region;

a first electrode which is electrically connected to said second semiconductor region in a region between a side wall spacer provided on a side wall of said projecting portion of said gate pillar and an adjacent side wall spacer;

a second electrode, formed on another major surface of said semiconductor main body, which is opposite to said major surface thereof; and

wherein said second electrode is made of either a metal layer in which nickel, titanium, nickel, and silver are sequentially stacked, or another metal layer in which titanium, nickel, and gold are sequentially stacked.

23. (New) The trench-gate type semiconductor device as claimed in claim 22, wherein said first electrode is a source electrode and said second electrode is a drain electrode.

24. (New) A trench-gate type semiconductor device, comprising:

a first conductivity type semiconductor main body;
a second conductivity type first semiconductor region formed at a predetermined depth within said semiconductor main body, said second conductivity type being opposite to said first conductivity type;

a first conductivity type second semiconductor region formed at a predetermined depth within said first semiconductor region;

a first trench which penetrates said first semiconductor region, said first trench extending from a

major surface of said second semiconductor region into said semiconductor main body;

a gate pillar, including portions of a conductive layer embedded via an insulating film into said first trench and a cap insulating film capping an upper surface of said conductive layer, said gate pillar having a portion projecting from the major surface of said second semiconductor region;

an electrode which is electrically connected to said second semiconductor region in a region between a side wall spacer provided on a side wall of said projecting portion of said gate pillar and an adjacent side wall spacer;

a field insulating film formed on a portion of the major surface of said semiconductor main body;

an extension portion of said conductive layer for said gate provided on a portion of said field insulating film;

an additional electrode made of the same material as that of said electrode and connected to said extension portion of said conductive layer for said gate; and

a back-to-back protective element, electrically connected between said electrode and said additional electrode, said back-to-back protective element being provided on another portion of said field insulating film.